SPECTRUM
SYSTEMENTWICKLUNG MICROELECTRONIC GMBH

# M3i.21xx - 8 bit transient recorder up to 1 GS/s

- **Up to 1 GS/s on one channel or 500 MS/s on two channels**
- **Simultaneously sampling on all channels**
- **Separate monolithic ADC and amplifier per channel**
- **8 input ranges: ±50 mV up to ±10 V**
- **Programmable input offset ±100%**
- **Up to 4 GSample (4 GByte) on-board memory**
- **256 MSample standard memory installed**
- **Window, re-arm, OR/AND trigger**
- **Synchronization of up to 8 cards per system**
- **Options: Multiple Recording, Timestamps**

| Speed | SNR | ENOB |
|---|---|---|
| 500 MS/s | up to 46.0 dB | up to 7.3 LSB |
| 1 GS/s | up to 44.9 dB | up to 7.2 LSB |


- 66 MHz 32 bit PCI-X interface
- 5V / 3.3V PCI compatible
- 100% compatible to conventional PCI > V2.1
- Sustained streaming mode up to 245 MB/s

- 2,5 GBit x1 PCIe Interface
- Works with x1/x4/x8/x16* PCIe slots
- Software compatible to PCI
- Sustained streaming mode up to 160 MB/s

| Operating Systems | Recomended Software | Drivers |
|---|---|---|
| • Windows 2k, XP, Vista, 7<br>• Linux Kernel 2.4 + 2.6<br>• Windows/Linux 32 and 64 bit | • Visual Basic, Visual C++, Borland C++ Builder, GNU C++, Borland Delphi, VB.NET, C#, J#, Python<br>• SBench 6 | • MATLAB<br>• LabVIEW<br>• LabWindows/CVI<br>• Agilent VEE |

| Model | 1 channel | 2 channels |
|---|---|---|
| M3i.2120 | 500 MS/s | |
| M3i.2122 | 500 MS/s | 250 MS/s |
| M3i.2130 | 1 GS/s | |
| M3i.2132 | 1 GS/s | 500 MS/s |

## General Information

The 4 models of the M3i.21xx series are designed for the very fast data acquisition. Each of the input channels has its own monolithic A/D converter and its own programmable input amplifier. This allows to record signals simultaneously on both channels with 8 bit resolution without any phase delay between them. The extremely large on-board memory allows long time recording even with the highest sampling rates. All boards of the M3i.21xx series may use the whole installed on-board memory for the currently activated number of channels. A FIFO mode is also integrated on the board. This allows the acquisition of data continuously for online processing or for data storage to hard disk.

*Some x16 PCIe slots are for the use of graphic cards only and can not be used for other cards.

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## Software Support

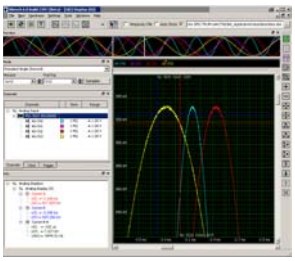
### Windows drivers

The cards are delivered with drivers for Windows 2000, XP, XP64, Vista and Vista64 as well as Windows 7. Programming examples for Visual C++, Borland C++ Builder, LabWindows/CVI, Borland Delphi, Visual Basic, VB.NET, C# and J# are included.

### Linux Drivers

All cards are delivered with full Linux support. Pre compiled kernel modules are included for the most common distributions like RedHat, Fedora, Suse or Debian. The Linux support includes SMP systems, 32 bit and 64 bit systems, versatile programming examples for Gnu C++ as well as the possibility to get the driver sources for own compilation.

### SBench 6



A base licence of SBench 6 the easy-to-use graphical operating software for the Spectrum cards is included in the delivery. Using the base license ist is possible to test the card and to show acquired data. There are also some basic measurement functions included in the base license. The card comes with a demo license for the professional version giving the user the oportunity to test the features of the professional version with the new hardware. Existing customers have the oportunity to request a demo license for the professional version at Spectrum. The professional version contains several new measurement functions, FFT, import and exporr (including MATLAB and ASCII) as well as the streaming modes. The data streaming modes allow to continuously acquire data to hard disk. SBench 6 has been optimized to handle data files of several GByte. More details on SBench 6 are found in the dedicated SBench 6 data shett. The version 6 is running under Windows as well as under Linux (KDE and GNOME). A test version of SBench 6 is freely available in the internet. This test version will also operate with demo cards and can be tested as Professional version without any hardware installed.

### Third-party products

A lot of third-party products are supported as an option. Choose between LabVIEW, MATLAB and Agilent VEE. All drivers come with examples and detailed documentation.

## Hardware features and options

### PCI/PCI-X

The cards with PCI/PCI-X bus connector use 32 Bit and up to 66 MHz clock rate for data transfer. They are 100% compatible to Conventional PCI > V2.1. The universal interface allows the use in PCI slots with 5 V I/O and 3.3 V I/O voltages as well as in PCI-X or PCI 64 slots. The maximum sustained data transfer rate is 245 MByte/s per bus segment.

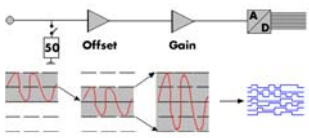
### PCI Express

The cards with PCI Express use a x1 PCIe connector. They can be used in PCI Express x1/x4/x8/x16 slots, except special graphic card slots, and are 100% software compatible to Conventional PCI > V2.1. The maximum sustained data transfer rate is 160 MByte/s per slot.

### SMA connectors

As an alternative to the standard SMB and MMCX connections the card can also be equipped with SMA connectors. The SMA connections are available for the analog input signals as well as for two of the additonal connections. These connections must be defined on the purchase order and can be a selection of: Trig-In, Trig-Out, Multi-Purpose X0, Clk-In, Clk-Out.

### Input Amplifier




The analog inputs can be adapted to real world signals using a wide variety of settings that are individual for each channel. By using software commands the input termination can be changed between 50 Ohm and 1 MOhm, one can select a matching input range and the signal offset can be compensated for.

### Software selectable input path

For each of the analog channels the user has the choice between two analog input paths, both offereing the highest flexibility when it comes to input ranges. The „Buffered" path has a fixed 1 MOhm termination, that allows to connect standard oscilloscope probes to the card. The „50 Ohm" path on the other hand provides the highest bandwith and the best signal integrity having a fixed 50 Ohm termination.

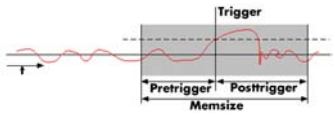
### Software selectable lowpass filter

Each analog channel contains a software selectable low-pass filter to limit the input bandwidth. Reducing the analog input bandwidth results in a lower total noise and can be usefull especially with low voltage input signals.

### Automatic on-board calibration

All of the channels are calibrated in factory before the board is shipped. To compensate for different variations like PC power supply, temperature and aging, the software driver provides routines for an automatic onboard offset and gain calibration of all input ranges of the „Buffered" path. All the cards contain a high precision on-board calibration reference.

### Ring buffer mode




The ring buffer mode is the standard mode of all oscilloscope boards. Data is written in a ring memory of the board until a trigger event is detected. After the event the posttrigger values are recorded. Because of this continuously recording into a ring buffer there are also samples prior to the trigger event visible: Pretrigger = Memsize - Posttrigger.

### FIFO mode

The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 245 MB/s on a PCI-X slot, up to 125 MB/s on a PCI slot and up to 160 MB/s on a PCIe slot) or hard disk. The control of the data stream is done automatically by the driver on interrupt request. The complete installed on-board memory is used for buffer data, making the continuous streaming extremely reliable.

### Channel trigger

The data acquisition boards offer a wide variety of trigger modes. Besides the standard signal checking for level and edge as known from oscilloscopes it's also possible to define a window trigger. All trigger modes can be combined with a re-arming mode (for accu-

rate trigger recognition on noisy signals) the AND/OR conjunction of different trigger events is possible.

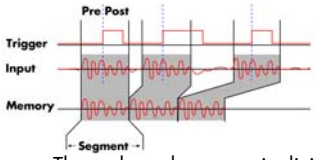
**External trigger input**

All boards can be triggered using an external analog or digital signal. It's possible to use positive or negative edge. As two analog comparators are used, one can also define a window trigger, a hysteresis trigger or a re-arm trigger.

**Universal Multi-Purpose I/Os**

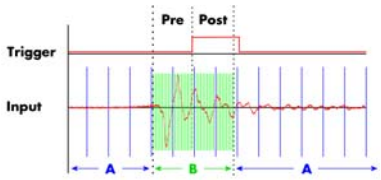

All M3i cards offer two universal multi-purpose I/O lines, which can be separately programmed as either input or output. These lines can be used as additional TTL trigger inputs for more complex trigger conditions. When used as outputs, these lines can be used to output card status signals like trigger-armed or to output the trigger to synchronize external equipment.

**Multiple Recording**



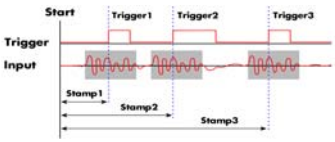

The Multiple Recording option allows the recording of several trigger events with an extremely short re-arming time. The hardware doesn't need to be restarted in between. The on-board memory is divided in several segments of the same size. Each of them is filled with data if a trigger event occurs. Pre- and posttrigger of the segments can be programmed. The number of acquired segments is only limited by the used memory and is unlimited when using FIFO mode.

**ABA mode**




The optional ABA mode combines slow continuous data recording with fast acquisition on trigger events. The ABA mode works like a slow data logger combined with a fast digitizer. The exact position of the trigger events is stored as timestamps in an extra memory.

**Timestamp**

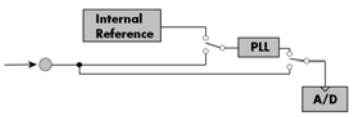



The timestamp option writes the time positions of the trigger events in an extra memory. The timestamps are relative to the start of recording, a defined zero time, externally synchronised to a radio clock, or a GPS receiver. With this option acquisitions of systems on different locations can be set in a precise time relation.

**External clock input and output**

Using a dedicated connector a sampling clock can be fed in from an external system. Additionally it's also possible to output the internally used sampling clock an a separate connector to synchronize external equipment to this clock.

**Reference clock**




The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronize the board for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

**Star-Hub**

The star-hub is an additional module allowing the phase stable synchronisation of up to 8 boards of a kind in one system. Independent of the number of boards there is no phase delay between all channels. The star-hub distributes trigger and clock information between all boards. As a result all connected boards are running with the same clock and the same trigger. All trigger sources can be combined with a logical OR allowing all channels of all cards to be trigger source at the same time.

**BaseXIO (enhanced timestamps)**

The BaseXIO option offers 8 asynchronous digital I/O lines on the base card, which are available on a separate bracket as SMB connectors. The direction can be selected by software in groups of four. In addition one of the I/O lines can be used as reference clock for the Timestamp counter.

**External Amplifiers**


For the acquisition of extremely small voltage levels with a high bandwidth a series of external amplifiers is available. Each of the one channel amplifiers is working with a fixed input impedanve and allows - depending on the bandwidth - to select different amplification levels between x10 (20 dB) up to x1000 (60 dB). Using the external amplifiers of the SPA series voltage levels in the uV and mV area can be acquired.

# Technical Data

**Analog Inputs**

| | |
|---|---|
| Resolution | 8 bit |
| Differential non linearity (DNL) | ≤ 0.6 LSB (ADC) |
| Integral non linearity (INL) | ≤ 1.0 LSB (ADC) |
| Programmable input offset | ± 100% of current input range |
| Connector (analog inputs) | 3 mm SMB male |
| Crosstalk sine signal ±1V, buffered path | -75 dB @ 100 MHz sine signal |
| Crosstalk sine signal ±1V , 50 ohm path | -75 dB @ 100 MHz sine signal |
| Crosstalk sine signal ±1V, 50 ohm path | -55 dB @ 250 MHz sine signal |
| 20 MHz BW Filter Characteristics | 3rd order Butterworth |

| **Input Path** | **50 ohm path 1** | **Buffered path 0** |
|---|---|---|
| Input impedance | fixed 50 Ohm | 50 Ohm, 1 MOhm\|\|25 pF |
| Max input @ 50 Ohm (> ±1 V range) | 5 Vrms | n.a. |
| Max input @ 50 Ohm (≤ ±1 V range) | 3.5 Vrms | n.a. |
| Max input @ 1 MOhm (> ±1 V range) | n.a. | ±30 V |
| Max input @ 1 MOhm (≤ ±1 V range) | n.a. | ±5 V |
| Max DC voltage if AC coupling active | ±30 V DC level | ±30 V DC level |
| Relative input stage delay | 0 ns | 2.5 ns |
| Input ranges | ±50 mV, ±100 mV, ±250 mV, ±500 mV, ±1 V, ±2 V, ±5 V, ±10 V | |
| Offset Error after warm-up + calibration | ≤0.5% of range | ≤0.5% of range |
| Gain Error after warm-up + calibration | ≤1.0% of range | ≤0.5% of range |

**Trigger**

| | |
|---|---|
| Multiple Recording: re-arming time | ≤ 64 Samples |
| Max Pretrigger at standard mode | up to full memsize |
| Max Pretrigger at Multi and FIFO | 16384 Samples as sum of all active channels |
| Internal trigger accuracy | 1 Sample |
| Channel trigger resolution | 8 bits |
| Trigger output delay | 261 sampling clock cycles (after trigger input) |
| External trigger type (Ext0) | Analog window comparator |
| Programmable trigger levels (Ext0) | 2 levels +/- 5V in steps of 1 mV |
| Minimum trigger pulse width | ≥ 2 clock periods |
| Ext. trigger connector (Ext0) | MMCX female |
| Ext. trigger max voltage 1 MOhm (Ext0) | ±30 V |
| Ext. trigger max voltage 50 Ohm (Ext0) | 5V rms |
| Ext. trigger impedance (Ext0) | 50 Ohm / 1 MOhm \|\| 25 pF |
| External trigger accuracy (All) | 2 Samples > 500 MS/s; 1 Sample (≤ 500 Ms/s) |
| Trigger output | see multi purpose I/O lines below |

| **Power consumption (max speed)** | **PCI / PCI-X** | | **PCI EXPRESS** | |
|---|---|---|---|---|
| | **3,3 V** | **5 V** | **3,3 V** | **12 V** |
| M3i.212x (256 MS memory) | 2.0 A | 2.3 A | 0.4 A | 1.9 A |
| M3i.21x2 (256 MS memory) | 2.3 A | 2.3 A | 0.4 A | 2.0 A |
| M3i.21x2 (4 GS memory), max. power | 2.4 A | 3.3 A | 0.4 A | 2.7 A |

| **Max channels with Star-Hub** | **SH4** | **SH8** |
|---|---|---|
| M3i.21x0 | 4 | 8 |
| M3i.21x2 | 8 | 16 |

**BaseXIO (Option)**

| | |
|---|---|
| BaseXIO Connector (extra bracket) | 8 x SMB male (8 x MMCX female internal) |
| BaseXIO input | TTL compatible: Low ≤ 0.8 V, High ≥ 2.0 V |
| BaseXIO input impedance | 4.7 kOhm towards 3.3 V |
| BaseXIO input maximum voltage | -0.5 V up to +5.5 V |
| BaseXIO output levels | TTL compatible: Low ≤ 0.4 V, High ≥ 2.4 V |
| BaseXIO output drive strength | 32 mA maximum current |

**Multi purpose digital I/O**

| | |
|---|---|
| No of multi purpose lines | two: (X0 = Ext1), (X1 = Ext2) |
| Connector Type | MMCX female |
| Input: available input signals | Additional TTL trigger, async input |
| Input: input impedance | 10 kOhm towards 3.3 V |
| Input: maximum voltage | -0.3 V up to +5.5 V |
| Input: input voltage level | Low ≤ 0.8 V, High ≥ 2.0 V |
| Input: minimum pulse width | ≥ 2 clock periods |
| | |
| Output: available output signals | trigger, arm, run, async output |
| Output: output impedance | 50 Ohm |
| Output: output levels (into high Z) | Low ≤ 0.4 V, High ≥ 2.4 V |
| Output: output type | TTL compatible for high-impedance loads |
| Output: output drive strength | Capable of driving 50 Ohm load |

**Clock**

| | |
|---|---|
| Internal clock range | 22.5 MHz to max (see table below) |
| Internal clock accuracy | max. ± 32 ppm |
| Internal clock setup granularity | 1 Hz |
| Clock range gaps (internal and external) | 70 to 72, 140 to 144, 281 to 287 MHz |
| External clock input connector/coupling | MMCX female, AC coupled |
| External clock input termination | 50 Ohm fixed |
| Reference clock: external clock range | ≥ 10.0 MHz and ≤ 1.0 GHz (fix @ runtime) |
| Sampling clock from ref clock range | 10 MHz to max (see table below) |
| Sampling clock from ref clock granularity | 1 kHz |
| External clock delay to internal ADC clock | 3.7 ns (8.2 ns at synchronized cards) |
| External clock input type | single-ended, sine wave or square wave |
| External clock min input swing | 0.3 V peak peak |
| External clock maximum voltage | 3.0 V peak peak |
| External clock duty cycle requirement | 40% to 60% |
| External clock output connector/coupling | MMCX female, AC coupled |
| External clock output type | single-ended, 3.3V LVPECL |
| External clock output drive strength | Capable of driving 50 ohm load |

**Environmental and Physical details**

| | |
|---|---|
| Dimension (PCB only) | 312 mm x 107 mm (full PCI length) |
| Width (Standard or star-hub 4) | 1 full size slot |
| Width (star-hub 8) | 2 full size slots |
| Width (with BaseXIO) | 1 full size slots + 1 half size slot |
| Weight (plain card) | 320 g |
| Weight (plain card + option SH4) | 380 g |
| Weight (plain card + option SH8) | 400 g |
| Warm up time | 10 minutes |
| Operating temperature | 0°C - 50°C |
| Storage temperature | -10°C - 70°C |
| Humidity | 10% to 90% |

**PCI / PCI-X specific details**

| | |
|---|---|
| PCI / PCI-X bus slot type | 32 bit 33/66 MHz |
| PCI / PCI-X bus slot compatibility | 32/64 bit, 33-133 MHz, 3,3 and 5 V I/O |

**PCI EXPRESS specific details**

| | |
|---|---|
| PCIe slot type | x1 |
| PCIe slot compatibility | x1/x4/x8/x16* |

*Some x16 PCIe slots are for graphic cards only and can not be used for other cards.

**Software programmable parameters**

| | |
|---|---|
| Input Ranges (Buffered path or 50 Ohm path) | ±50mV, ±100mV, ±250mV, ±500mV, ±1V, ±2V, ±5V, ±10V |
| Analog input impedance | 50 Ohm / 1M Ohm |
| Analog input coupling | AC / DC |
| Analog bandwidth limit filter | on/off |
| Clock mode | Internal, external reference clock, sync |
| External trigger impedance | 50 Ohm / 1 MOhm |
| External trigger coupling | AC / DC |
| Trigger mode | Ch0, Ch1, Ext0(Analog), Ext1/2(TTL), SW |
| Enhanced trigger | Window, Re-Arm, Or/And, Delay |
| Trigger level (channel) | 8 bit resolution relating to input range |
| Trigger level (Ext0) | 1 mV resolution: -5000 mV to +5000 mV |
| Trigger edge (channel + external) | Rising edge, falling edge or both edges |
| Trigger delay | 0 to 64G samples in steps of 16 samples |
| External trigger (Ext0) coupling | AC/DC |
| External trigger (Ext0) impedance | 50 Ohm / 1M Ohm |
| Memory depth | 32 up to [installed memory / number of active channels] in steps of 16 |
| Posttrigger | 16 up to 8 GSamples in steps of 16 |
| Multiple Recording segment size | 32 up to[installed memory / 2 / active channels] in steps of 32 |
| Multiple Recording pretrigger | 16 up to [16k samples / number of active channels] |

**Certifications, Compliances, Warranty**

| | |
|---|---|
| EMC Immunity | Compliant with CE Mark |
| EMC Emission | Compliant with CE Mark |
| Product warranty | 2 years starting with the day of delivery |
| Software and firmware updates | Life-time, free of charge |

**Option SMA connectors**

| | |
|---|---|
| Available signals for SMA XA | One of Trig-In, Trig-Out, Multi Purpose X0 |
| Available signals for SMA XB | One of Clk-In, Clk-Out, Trig-In |

| | M3i.2120 | M3i.2122 | M3i.2130 | M3i.2132 |
|---|---|---|---|---|
| max internal clock (1 channel active) | 500 MS/s | 500 MS/s | 1 GS/s | 1 GS/s |
| max internal clock (2 channels active) | n.a. | 250 MS/s | n.a. | 500 MS/s |
| lower bandwidth limit (DC coupling) | 0 Hz | 0 Hz | 0 Hz | 0 Hz |
| lower bandwidth limit (AC coupled, 50 Ohm) | <30 kHz | <30 kHz | <30 kHz | <30 kHz |
| lower bandwidth limit (AC coupled, 1 MOhm) | <2 Hz | <2 Hz | <2 Hz | <2 Hz |
| -3 dB bandwidth (buffered path) | 150 MHz | 150 MHz | 200 MHz | 200 MHz |
| -3 dB bandwidth (50 ohm path) | 250 MHz | 250 MHz | 500 MHz | 500 MHz |
| -3 dB bandwidth (BW limit enabled) | 20 MHz | 20 MHz | 20 MHz | 20 MHz |

## Dynamic Parameters

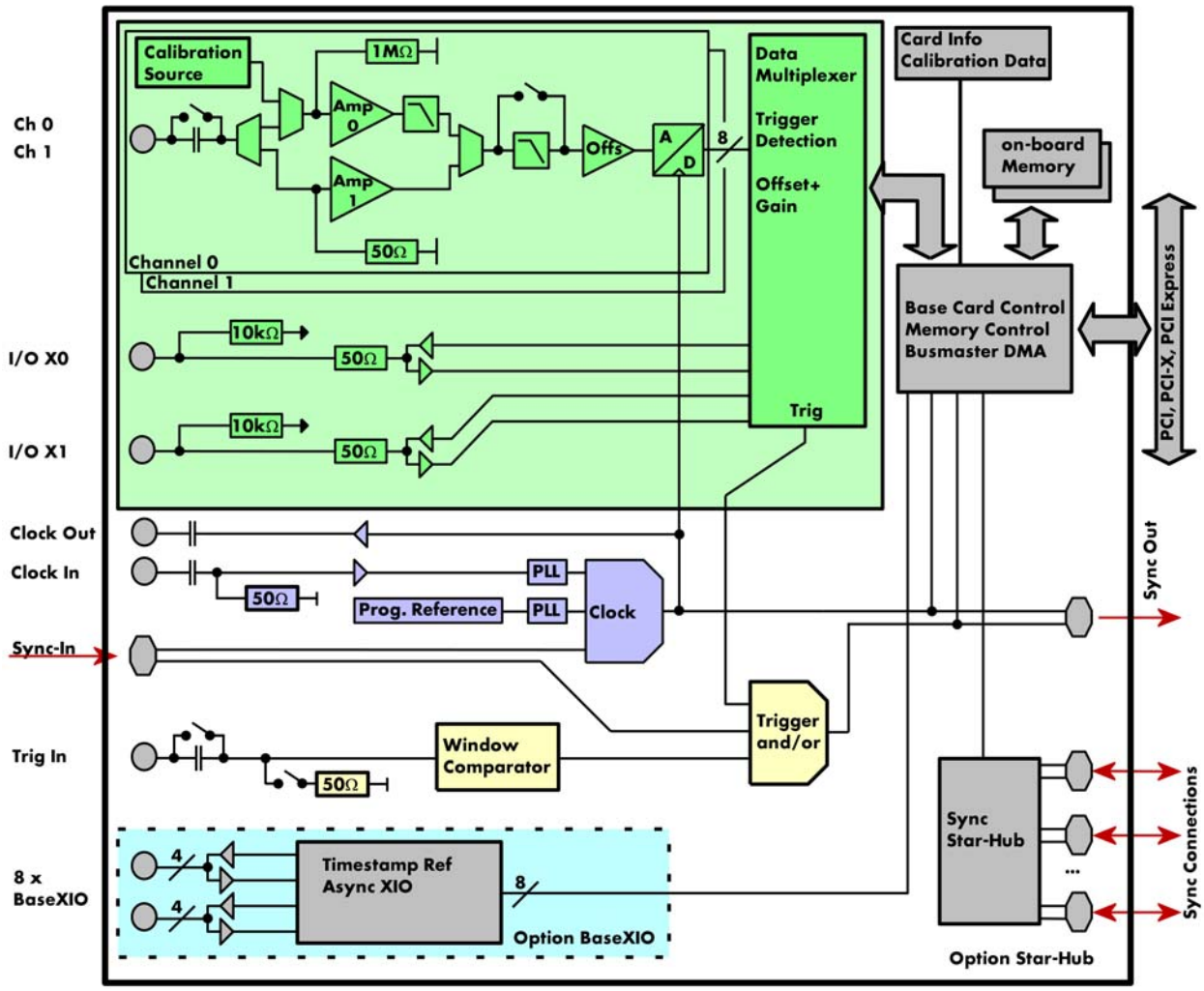
| | M3i.2130 and M3i.2132, 1 channel 1 GS/s (bandwidth 500 MHz) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Input Path | HF path, AC coupled, fixed 50 Ohm, full BW | | | | | | Buffered path, BW limit | | | Buffered path, full BW | | |
| Test signal frequency | 9 MHz | | | | 40 MHz | 70 MHz | 9 MHz | | | 9 MHz | 40 MHz | 70 MHz |
| Input Range | ±50mV | ±100mV | ±250mV | ±500mV | ±500mV | ±500mV | ±50mV | ±250mV | ±1V | ±500mV | ±500mV | ±500mV |
| RMS Noise (zero level) | <0.5 | | | | | | <0.6 | <0.5 | <0.5 | <0.4 | | |
| THD (typ) (dB | 54.1 | 54.0 | 54.1 | 54.2 | 54.2 | 54.3 | 53.8 | 54.1 | 53.8 | 54.1 | 54.4 | 52.5 |
| SNR (typ) (dB) | 44.5 | 44.8 | 44.9 | 44.9 | 44.7 | 44.6 | 44.3 | 44.6 | 43.5 | 44.4 | 44.7 | 43.9 |
| SFDR (typ), excl. harm. (dB) | 62.4 | 63.4 | 64.3 | 62.7 | 59,5 | 56.4 | 62.1 | 62.9 | 50.7 | 53.1 | 54.5 | 52.2 |
| SFDR (typ), incl. harm. (dB) | 55.3 | 55.2 | 55.1 | 55.3 | 55.8 | 56.2 | 55.4 | 55.0 | 50.6 | 53.0 | 54.3 | 52.1 |
| SINAD/THD+N (typ) (dB) | 44.0 | 44.2 | 44.2 | 44.2 | 44.2 | 44.1 | 43.9 | 44.1 | 43.0 | 43.9 | 44.1 | 43.4 |
| ENOB based on SINAD (bit) | 7.0 | 7.1 | 7.1 | 7.1 | 7.0 | 7.0 | 7.0 | 7.0 | 6.9 | 7.0 | 7.0 | 6.9 |
| ENOB based on SNR (bit) | 7.1 | 7.1 | 7.2 | 7.2 | 7.1 | 7.1 | 7.1 | 7.1 | 6.9 | 7.1 | 7.1 | 7.0 |

| | M3i.2132, 2 channels 500 MS/s (bandwidth 500 MHz) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Input Path | HF path, AC coupled, fixed 50 Ohm, full BW | | | | | | Buffered path, BW limit | | | Buffered path, full BW | | |
| Test signal frequency | 9 MHz | | | | 40 MHz | 70 MHz | 9 MHz | | | 9 MHz | 40 MHz | 70 MHz |
| Input Range | ±50mV | ±100mV | ±250mV | ±500mV | ±500mV | ±500mV | ±50mV | ±250mV | ±1V | ±500mV | ±500mV | ±500mV |
| RMS Noise (zero level) | <0.5 | | | | | | <0.6 | <0.5 | <0.5 | <0.5 | | |
| THD (typ) (dB | 55.5 | 55.6 | 55.4 | 55.5 | 55.1 | 54.9 | 54.7 | 55.1 | 55.0 | 55.4 | 55.6 | 53.0 |
| SNR (typ) (dB) | 44.6 | 45.1 | 45.0 | 45.1 | 45.0 | 44.9 | 44.7 | 45.0 | 44.7 | 44.9 | 45.2 | 45.3 |
| SFDR (typ), excl. harm. (dB) | 64.5 | 65.5 | 64.3 | 65.6 | 65.3 | 62.3 | 64.0 | 64.9 | 65.2 | 65.4 | 64.7 | 64.9 |
| SFDR (typ), incl. harm. (dB) | 58.8 | 58.9 | 58.8 | 59.0 | 58.5 | 56.7 | 57.9 | 58.1 | 58.3 | 58.2 | 58.9 | 56.3 |
| SINAD/THD+N (typ) (dB) | 44.3 | 44.8 | 44.6 | 44.7 | 44.6 | 44.4 | 44.3 | 44.6 | 44.3 | 44.9 | 44.8 | 44.6 |
| ENOB based on SINAD (bit) | 7.0 | 7.1 | 7.1 | 7.1 | 7.1 | 7.1 | 7.0 | 7.1 | 7.1 | 7.2 | 7.1 | 7.1 |
| ENOB based on SNR (bit) | 7.1 | 7.2 | 7.2 | 7.2 | 7.2 | 7.1 | 7.1 | 7.2 | 7.1 | 7.2 | 7.2 | 7.2 |

| | M3i.2120 and M3i.2122, 1 channel 500 MS/s or 2 channels 250 MS/s (bandwidth 250 MHz) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Input Path | HF path, AC coupled, fixed 50 Ohm, full BW | | | | | | Buffered path, BW limit | | | Buffered path, full BW | | |
| Test signal frequency | 9 MHz | | | | 40 MHz | 70 MHz | 9 MHz | | | 9 MHz | 40 MHz | 70 MHz |
| Input Range | ±50mV | ±100mV | ±250mV | ±500mV | ±500mV | ±500mV | ±50mV | ±250mV | ±1V | ±500mV | ±500mV | ±500mV |
| RMS Noise (zero level) (LSB) | <0.4 | | | | | | <0.5 | <0.4 | <0.5 | <0.4 | | |
| THD (typ) (dB | 52.7 | 52.8 | 52.5 | 53.1 | 51.7 | 52.8 | 53.0 | 53.3 | 53.1 | 53.1 | 62.4 | 50.4 |
| SNR (typ) (dB) | 45.7 | 45.9 | 45.9 | 46.0 | 46.1 | 45.8 | 45.1 | 45.6 | 45.0 | 45.7 | 45.7 | 45.4 |
| SFDR (typ), excl. harm. (dB) | 61.3 | 61.0 | 63.0 | 61.2 | 64.4 | 60.8 | 60.2 | 61.5 | 60.5 | 61.4 | 63.5 | 60.3 |
| SFDR (typ), incl. harm. (dB) | 52.7 | 52.6 | 52.5 | 52.8 | 52.6 | 53.7 | 53.3 | 53.2 | 53.0 | 53.0 | 53.3 | 53.0 |
| SINAD/THD+N (typ) (dB) | 45.0 | 45.1 | 45.0 | 45.2 | 45.0 | 45.0 | 44.5 | 45.0 | 44.4 | 44.4 | 44.8 | 44.2 |
| ENOB based on SINAD (bit) | 7.2 | 7.2 | 7.2 | 7.2 | 7.2 | 7.2 | 7.1 | 7.2 | 7.1 | 7.2 | 7.2 | 7.1 |
| ENOB based on SNR (bit) | 7.3 | 7.3 | 7.3 | 7.3 | 7.3 | 7.3 | 7.2 | 7.3 | 7.2 | 7.3 | 7.3 | 7.3 |

A pure sine wave with > 99% amplitude of input range is measured with 50 ohms termination. SNR and RMS noise parameters may differ depending on the quality of the used PC. SNR = Signal to Noise Ratio, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range, SINAD = Signal Noise and Distortion, ENOB = Effective Number of Bits. For a detailed description please see application note 002.

## Hardware block diagram



# Order Information

## PCI/PCI-X

| Order no. | Standard mem | 1 channel | 2 channels |
|---|---|---|---|
| M3i.2120 | 256 MByte | 500 MS/s | |
| M3i.2122 | 256 MByte | 500 MS/s | 250 MS/s |
| M3i.2130 | 256 MByte | 1 GS/s | |
| M3i.2132 | 256 MByte | 1 GS/s | 500 MS/s |

## PCI Express

| Order no. | Standard mem | 1 channel | 2 channels |
|---|---|---|---|
| M3i.2120-exp | 256 MByte | 500 MS/s | |
| M3i.2122-exp | 256 MByte | 500 MS/s | 250 MS/s |
| M3i.2130-exp | 256 MByte | 1 GS/s | |
| M3i.2132-exp | 256 MByte | 1 GS/s | 500 MS/s |

## Memory

| Order no. | Option |
|---|---|
| M3i.xxxx-512MB | Memory upgrade to 512 MB of total memory |
| M3i.xxxx-1GB | Memory upgrade to 1 GB of total memory |
| M3i.xxxx-2GB | Memory upgrade to 2 GB of total memory |
| M3i.xxxx-4GB | Memory upgrade to 4 GB of total memory |

## Options

| Order no. | Option |
|---|---|
| M3i.xxxx-mr | Option Multiple Recording |
| M3i.xxxx-mt | Option pack including Multiple Recording, Timestamp |
| M3i.xxxx-mtab | Option pack including Multiple Recording, Timestamp, ABA mode |
| M3i.xxxx-SH4 | Synchronization Star-Hub for up to 4 cards, only 1 slot width |
| M3i.xxxx-SH8 | Synchronization Star-Hub for up to 8 cards, 2 slots width |
| M3i.xxxx-bxio | Option BaseXIO: 8 digital I/O lines usable as asynchronous I/O and timestamp ref-clock, additional bracket with 8 SMB connectors |
| M3i.xxxx-SMA | Option SMA connections for analog inputs + two signals of Clock-In, Clock-Out, Trig-In, Trig-Out, X0 |
| M3i-upgrade | Upgrade for M3i.xxxx: later installation of option -bxio or SMA connectors |

## Cables

| | | | Order no. | | | |
|---|---|---|---|---|---|---|
| for Connections | Connection | Length | to BNC male | to BNC female | to SMA male | to SMA female |
| Standard inputs | SMB female | 80 cm | Cab-3f-9m-80 | Cab-3f-9f-80 | Cab-3f-3mA-80 | Cab-3f-3fA-80 |
| Standard inputs | SMB female | 200 cm | Cab-3f-9m-200 | Cab-3f-9f-200 | Cab-3f-3mA-200 | Cab-3f-3fA-200 |
| Probes (short) | SMB female | 5 cm | | Cab-3f-9f-5 | | |
| Trigger/Clock/Extra | MMCX male | 80 cm | Cab-1m-9m-80 | Cab-1m-9f-80 | Cab-1m-3mA-80 | Cab-1m-3fA-80 |
| Trigger/Clock/Extra | MMCX male | 200 cm | Cab-1m-9m-200 | Cab-1m-9f200 | Cab-1m-3mA-200 | Cab-1m-3fA-200 |
| SMA Option | SMA male | 80 cm | Cab-3mA-9m-80 | Cab-3mA-9f-80 | | |
| SMA Option | SMA male | 200 cm | Cab-3mA-9m-200 | Cab-3mA-9f-200 | | |

## Amplifiers

| Order no. | Bandwidth | Input Impedance | Coupling | Amplification |
|---|---|---|---|---|
| SPA.1601 (2) | 500 MHz | 50 Ohm | DC | x10 (20 dB) |
| SPA.1412 (2) | 200 MHz | 1 MOhm | AC/DC | x10/x100 (20/40 dB) |
| SPA.1411 (2) | 200 MHz | 50 Ohm | AC/DC | x10/x100 (20/40 dB) |
| SPA.1232 (2) | 10 MHz | 1 MOhm | AC/DC | x100/x1000 (40/60 dB) |
| SPA.1231 (2) | 10 MHz | 50 Ohm | AC/DC | x100/x1000 (40/60 dB) |
| SPA.PW1-120 (2) | External power supply for all SPA amplifiers with 120 VAC, type A (US, Japan) connector | | | |
| SPA.PW1-230 (2) | External power supply for all SPA amplifiers with 230 VAC, type C (European) connector | | | |
| Information | External Amplifiers with one channel, BNC connections, manually adjustable offset, manually switch between settings. A power supply need to be ordered for each amplifier! | | | |

## Drivers

| Order no. | Option |
|---|---|
| M3i.xxxx-ml | MATLAB driver for all M3i and M3i Express cards |
| M3i.xxxx-lv | LabVIEW driver for all M3i and M3i Express cards |
| M3i.21xx-vee | Agilent VEE driver for all M3i.21xx cards |

## SBench6

| Order no. | |
|---|---|
| SBench6 | Base version which support standard mode for one card |
| SBench6-Pro | Professional version for one card: FIFO mode, export/import, calculation functions |
| SBench6-Multi | Option multiple cards: needs Professional version. Handles multiple synchronized cards in one system. |
| Volume Licenses | Please ask Spectrum for details. |

*(1) : Just one of the options can be installed on a card at a time.*
*(2) : Third party product with warranty differing from our export conditions. No volume rebate possible.*

**Technical changes and printing errors possible**