

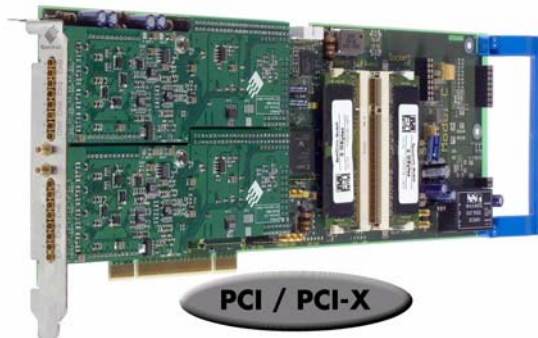


SPECTRUM

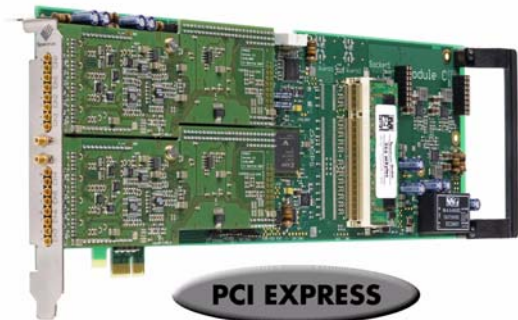
SYSTEMENTWICKLUNG MICROELECTRONIC GMBH

M2i.46xx - 8 channel 16 bit A/D up to 3 MS/s

- 2, 4 or 8 channels with 200 kS/s up to 3 MS/s
- Simultaneously sampling on all channels
- Software selectable single-ended or differential inputs
- Separate ADC and amplifier per channel
- complete on-board calibration
- 8 input ranges: ± 50 mV up to ± 10 V
- Up to 2 GSample on-board memory
- 128 MSample standard on-board memory
- Window, pulse width, re-arm, spike, OR/AND trigger
- Programmable input offset of ± 5 V
- Synchronization of up to 16 cards per system and up to 271 cards with system sync
- Options: ABA mode, Multiple Recording, Gated Sampling, BaseXIO



PCI / PCI-X



PCI EXPRESS

- 66 MHz 32 bit PCI-X interface
- 5V / 3.3V PCI compatible
- 100% compatible to conventional PCI > V2.1
- Sustained streaming mode up to 245 MB/s

- 2,5 GBit x1 PCIe Interface
- Works with x1/x4/x8/x16* PCIe slots
- Software compatible to PCI
- Sustained streaming mode up to 160 MB/s

Operating Systems	Recommended Software	Drivers
<ul style="list-style-type: none"> • Windows 2k, XP, Vista, 7 • Linux Kernel 2.4 + 2.6 • Windows/Linux 32 and 64 bit 	<ul style="list-style-type: none"> • Visual Basic, Visual C++, Borland C++ Builder, GNU C++, Borland Delphi, .VB.NET, C#, J#, Python • SBench 6 	<ul style="list-style-type: none"> • MATLAB • LabVIEW, LabWindows • DASYLab • Agilent VEE

Model	1 channel	2 channels	4 channels	8 channels
M2i.4620	200 kS/s	200 kS/s		
M2i.4621	200 kS/s	200 kS/s	200 kS/s	
M2i.4622	200 kS/s	200 kS/s	200 kS/s	200 kS/s
M2i.4630	500 kS/s	500 kS/s		
M2i.4631	500 kS/s	500 kS/s	500 kS/s	
M2i.4632	500 kS/s	500 kS/s	500 kS/s	500 kS/s
M2i.4640	1 MS/s	1 MS/s		
M2i.4641	1 MS/s	1 MS/s	1 MS/s	
M2i.4642	1 MS/s	1 MS/s	1 MS/s	1 MS/s
M2i.4650	3 MS/s	3 MS/s		
M2i.4651	3 MS/s	3 MS/s	3 MS/s	
M2i.4652	3 MS/s	3 MS/s	3 MS/s	3 MS/s

General Information

The M2i.46xx series allows recording of one, two, four or eight channels with sampling rates of 200 kS/s up to 3 MS/s. These cards offer outstanding A/D features both in resolution and speed for PCI/PCI-X and PCI Express. They are available in several versions and different speed grades making it possible for the user to find an individual solution. All boards of the M2i.46xx series may use the whole installed on-board memory, of up to 2 GSamples, completely for the currently activated number of channels. The enhanced FIFO engine is capable of streaming even 8 channels with 3 MS/s sustained to memory or hard disk.

*Some x16 PCIe slots are for the use of graphic cards only and can not be used for other cards.

Software Support

Windows drivers

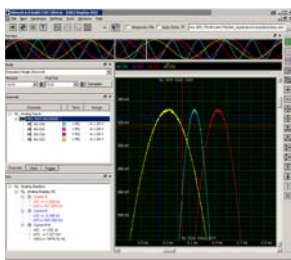
The cards are delivered with drivers for Windows 2000, XP, XP64, Vista and Vista64 as well as Windows 7. Programming examples for Visual C++, Borland C++ Builder, LabWindows/CVI, Borland Delphi, Visual Basic, VB.NET, C# and J# are included.

Linux Drivers



All cards are delivered with full Linux support. Pre compiled kernel modules are included for the most common distributions like RedHat, Fedora, Suse or Debian. The Linux support includes SMP systems, 32 bit and 64 bit systems, versatile programming examples for Gnu C++ as well as the possibility to get the driver sources for own compilation.

SBench 6



A base licence of SBench 6 the easy-to-use graphical operating software for the Spectrum cards is included in the delivery. Using the base license it is possible to test the card and to show acquired data. There are also some basic measurement functions included in the base license. The card comes with a demo license for the professional

version giving the user the opportunity to test the features of the professional version with the new hardware. Existing customers have the opportunity to request a demo license for the professional version at Spectrum. The professional version contains several new measurement functions, FFT, import and export (including MATLAB and ASCII) as well as the streaming modes. The data streaming modes allow to continuously acquire data to hard disk. SBench 6 has been optimized to handle data files of several GByte. More details on SBench 6 are found in the dedicated SBench 6 data sheet. The version 6 is running under Windows as well as under Linux (KDE and GNOME). A test version of SBench 6 is freely available in the internet. This test version will also operate with demo cards and can be tested as Professional version without any hardware installed.

Third-party products

A lot of third-party products are supported as an option. Choose between LabVIEW, MATLAB, DASyLab and Agilent VEE. All drivers come with examples and detailed documentation.

Hardware features and options

PCI/PCI-X



The cards with PCI/PCI-X bus connector use 32 Bit and up to 66 MHz clock rate for data transfer. They are 100% compatible to Conventional PCI > V2.1. The universal interface allows the use in PCI slots with 5 V I/O and 3.3 V I/O voltages as well as in PCI

X or PCI 64 slots. The maximum sustained data transfer rate is 245 MByte/s per bus segment.

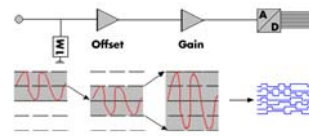
PCI Express



The cards with PCI Express use a x1 PCIe connector. They can be used in PCI Express x1/x4/x8/x16 slots, except special graphic card slots, and are 100% software compatible to

Conventional PCI > V2.1. The maximum sustained data transfer rate is 160 MByte/s per slot.

Input Amplifier



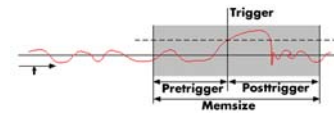
The analog inputs can be adapted to real world signals using a wide variety of settings that are individual for each channel. By using software commands one can select a matching input range

and the signal offset can be compensated.

Differential inputs

With a simple software command the inputs can individually be switched from single-ended (in relation to ground) to differential, without losing any inputs. When the inputs are used in differential mode the A/D converter measures the difference between two lines with relation to system ground.

Ring buffer mode



The ring buffer mode is the standard mode of all oscilloscope boards. Data is written in a ring memory of the board until a trigger event is

detected. After the event the posttrigger values are recorded. Because of this continuously recording into a ring buffer there are also samples prior to the trigger event visible: Pretrigger = Memsize - Posttrigger.

FIFO mode

The FIFO mode is designed for continuous data transfer between measurement board and PC memory (up to 245 MB/s on a PCI-X slot, up to 125 MB/s on a PCI slot and up to 160 MB/s on a PCIe slot) or hard disk. The control of the data stream is done automatically by the driver on interrupt request. The complete installed on-board memory is used for buffer data, making the continuous streaming extremely reliable.

Channel trigger

The data acquisition boards offer a wide variety of trigger modes. Besides the standard signal checking for level and edge as known from oscilloscopes it's also possible to define a window trigger. All trigger modes can be combined with the pulsewidth trigger. This makes it possible to trigger on signal errors like too long or too short pulses. In addition to this a re-arming mode (for accurate trigger recognition on noisy signals) the AND/OR conjunction of different trigger events is possible. As a unique feature it is possible to use deactivated channels as trigger sources.

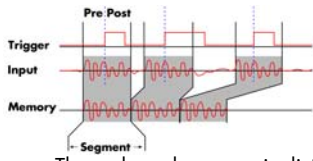
External trigger I/O

All boards can be triggered using an external TTL signal. It's possible to use positive or negative edge also in combination with a programmable pulse width. An internally recognised trigger event can - when activated by software - be routed to the trigger connector to start external instruments.

Pulse width

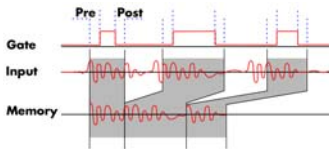
Defines the minimum or maximum width that a trigger pulse must have to generate a trigger event. Pulse width can be combined with channel trigger, pattern trigger and external trigger.

Multiple Recording



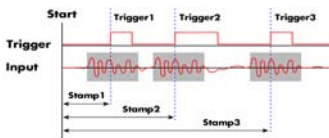
The Multiple Recording option allows the recording of several trigger events with an extremely short re-arming time. The hardware doesn't need to be restarted in between. The on-board memory is divided in several segments of the same size. Each of them is filled with data if a trigger event occurs. Pre- and posttrigger of the segments can be programmed. The number of acquired segments is only limited by the used memory and is unlimited when using FIFO mode.

Gated Sampling



The Gated Sampling option allows data recording controlled by an external gate signal. Data is only recorded if the gate signal has a programmed level. In addition a pre-area before start of the gate signal as well as a post area after end of the gate signal can be acquired. The number of gate segments is only limited by the used memory and is unlimited when using FIFO mode.

Timestamp

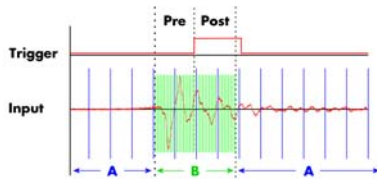


The timestamp option writes the time positions of the trigger events in an extra memory. The timestamps are relative to the start of recording, a defined zero time, externally synchronised to a radio clock, or a GPS receiver. With this option acquisitions of systems on different locations can be set in a precise time relation.

External clock I/O

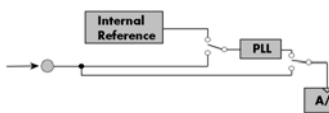
Using a dedicated connector a sampling clock can be fed in from an external system. It's also possible to output the internally used sampling clock to synchronise external equipment to this clock.

ABA mode



The optional ABA mode combines slow continuous data recording with fast acquisition on trigger events. The ABA mode works like a slow data logger combined with a fast digitizer. The exact position of the trigger events is stored as timestamps in an extra memory.

Reference clock



The option to use a precise external reference clock (normally 10 MHz) is necessary to synchronize the board for high-quality measurements with external equipment (like a signal source). It's also possible to enhance the quality of the sampling clock in this way. The driver automatically generates the requested sampling clock from the fed in reference clock.

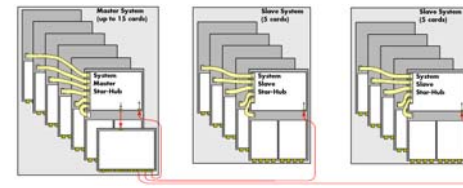
Star-Hub



The star-hub is an additional module allowing the phase stable synchronisation of up to 16 boards in one system. Independent of the number of boards there is no phase delay between all channels. The star-hub distributes trigger and

clock information between all boards. As a result all connected boards are running with the same clock and the same trigger. All trigger sources can be combined with OR/AND allowing all channels of all cards to be trigger source at the same time. The star-hub is available as 5 card and 16 card version. The 5 card version doesn't need an extra slot.

271 synchronous cards with the System Star-Hub



With the help of multiple system star-hubs it is possible to link up to 17 system phase synchronous with each other.

Each system can then contain up to 16 cards (master only 15). In total 271 cards can be used fully synchronously in a bunch of systems. One master system distributes clock and trigger signal to all connected slave systems.

BaseXIO (enhanced trigger)



The BaseXIO option offers 8 asynchronous digital I/O lines on the base card. The direction can be selected by software in groups of four. Two of these lines can also be used as additional external trigger sources.

This allows the building of complex trigger conjunctions with external gated triggers as well as AND/OR conjunction of multiple external trigger sources like, for example, the picture and row synchronisation of video signals. In addition one of the I/O lines can be used as reference clock for the Timestamp counter.

Technical Data

Analog Inputs

Resolution	16 bit (± 32000 values)
ADC Differential non linearity (DNL)	465x: ± 2 LSB, all others ± 1 LSB
ADC Integral non linearity (INL)	465x: ± 2 LSB, all others ± 1 LSB
Offset error (full speed)	$\leq 0.1\%$ of range ± 0.2 mV (after warm-up/calibration)
Gain error (full speed)	$\leq 0.1\%$ (after warm-up and calibration)
Programmable input offset	± 5 V for single-ended ranges $< \pm 10$ V
Crosstalk: all ranges 100 kHz signal	≤ -110 dB on adjacent channels, 50 ohm term.
Analog Input impedance	1 MOhm against GND
Over voltage protection	± 30 V all ranges (activated card)
CMRR for ± 50 mV to ± 500 mV	> 70 dB
CMRR for ± 1 V to ± 10 V	> 46 dB
Connector (analog)	MMCX female
Connector (trigger/clock)	3 mm SMB male

Trigger

Multi, Gate: re-arming time	< 4 samples
Max Pretrigger at Multi, Gate, FIFO	8176 Samples as sum of all active channels
Internal/External trigger accuracy	1 Sample
Channel trigger resolution	14 bit
Trigger output delay	One positive edge after internal trigger event
External trigger type	3.3V LVTTTL compatible (5V tolerant)
External trigger input	Low ≤ 0.8 V, High ≥ 2.0 V, ≥ 8 ns in pulse stretch mode, ≥ 2 clock periods all other modes
External trigger maximum voltage	-0.5 V up to +5.7 V (internally clamped to 5.0V, 100 mA max. clamping current)
External trigger output levels	Low ≤ 0.4 V, High ≥ 2.4 V, TTL compatible
External trigger output drive strength	Capable of driving 50 ohm load

Environmental and Physical details

Dimension (PCB only)	312 mm x 107 mm (full PCI length)
Width (Standard or star-hub 5)	1 full size slot
Width (star-hub 16)	2 full size slots
Weight (depending on options/channels)	290g (2/4 ch) up to 460g (8 ch + star-hub)
Warm up time	10 minutes
Operating temperature	0°C - 50°C
Storage temperature	-10°C - 70°C
Humidity	10% to 90%

PCI / PCI-X specific details

PCI / PCI-X bus slot type	32 bit 33/66 MHz
PCI / PCI-X bus slot compatibility	32/64 bit, 33-133 MHz, 3,3 V and 5 V I/O

PCI EXPRESS specific details

PCIe slot type	x1
PCIe slot compatibility	x1/x4/x8/x16*

*Some x16 PCIe slots are for graphic cards only and can not be used for other cards.

Power consumption (max speed)	PCI / PCI-X		PCI EXPRESS	
	3,3 V	5 V	3,3 V	12 V
M2i.46x0 (128 MS memory)	1.9 A	0.6 A	0.4 A	0.9 A
M2i.46x1 (128 MS memory)	1.9 A	1.0 A	0.4 A	1.1 A
M2i.46x2 (128 MS memory)	2.0 A	1.9 A	0.4 A	1.5 A
M2i.4652 (2 GS memory), max power	3.1 A	1.9 A	0.4 A	2.1 A

Max channels with Star-Hub	SH5	SH16	SSH55	SSH516
M2i.46x0	10	32	170	542
M2i.46x1	20	64	340	1084
M2i.46x2	40	128	680	2168

Clock

Internal clock range (PLL mode)	1 kS/s to max (see table below)
Internal clock accuracy	≤ 20 ppm
Internal clock: max. jitter in PLL mode	TBD
Internal clock: max. jitter in quartz mode	TBD
Internal clock setup granularity	$\leq 1\%$ of range (100M, 10M, 1M, 100k,...)
Internal clock setup granularity example	range 1M to 10M: stepsize ≤ 100 k
Reference clock: external clock range	≥ 1.0 MHz and ≤ 125.0 MHz
External clock range	see table below
External clock delay to internal clock	5.4 ns
External clock type/edge	3.3V LVTTTL compatible, rising edge used
External clock input	Low ≤ 0.8 V, High ≥ 2.0 V, duty 45% - 55%
External clock maximum voltage	-0.5 V up to +3.8 V (internally clamped to 3.3V, 100 mA max. clamping current)
External clock output levels	Low ≤ 0.4 V, High ≥ 2.4 V, TTL compatible
External clock output drive strength	Capable of driving 50 ohm load

BaseXIO (Option)

BaseXIO Connector (extra bracket)	8 x SMB (8 x MMCX internal)
BaseXIO input	TTL compatible: Low ≤ 0.8 V, High ≥ 2.0 V
BaseXIO input impedance	4.7 kOhm towards 3.3 V
BaseXIO input maximum voltage	-0.5 V up to +5.5 V
BaseXIO output levels	TTL compatible: Low ≤ 0.4 V, High ≥ 2.4 V
BaseXIO output drive strength	32 mA maximum current

Software programmable parameters

Input Range	± 50 mV, ± 100 mV, ± 250 mV, ± 500 mV, ± 1 V, ± 2 V, ± 5 V, ± 10 V
Input Offset (single-ended)	programmable to ± 5 V in steps of 1 mV, not exceeding ± 10 V input
Input type	Single-ended, true differential
Clock mode	Int. PLL, int. quartz, ext. clock, ext. divided, ext. reference clock, sync
Clock impedance	50 Ohm / high impedance (> 4 kOhm)
Trigger impedance	50 Ohm / high impedance (> 4 kOhm)
Trigger mode	Channel, Extern, SW, Auto, Window, Pulse, Re-Arm, Or/And, Delay
Trigger level resolution	14 bit
Trigger edge	Rising edge, falling edge or both edges
Trigger pulse width	0 to [64k - 1] samples in steps of 1 sample
Trigger delay	0 to [64k - 1] samples in steps of 1 sample
Memory depth	8 up to [installed memory / number of active channels] samples in steps of 4
Posttrigger	4 up to [8G - 4] samples in steps of 4
Multiple Recording segment size	8 up to [installed memory / 2 / active channels] samples in steps of 4
Multi / Gated pretrigger	0 up to [8k samples / number of active channels - 16]
ABA clock divider	1 up to [64k - 1] in steps of 1
Synchronization clock divider	2 up to [8k - 2] in steps of 2
Channel selection	1, 2, 4 or 8 channels

Certifications, Compliances, Warranty

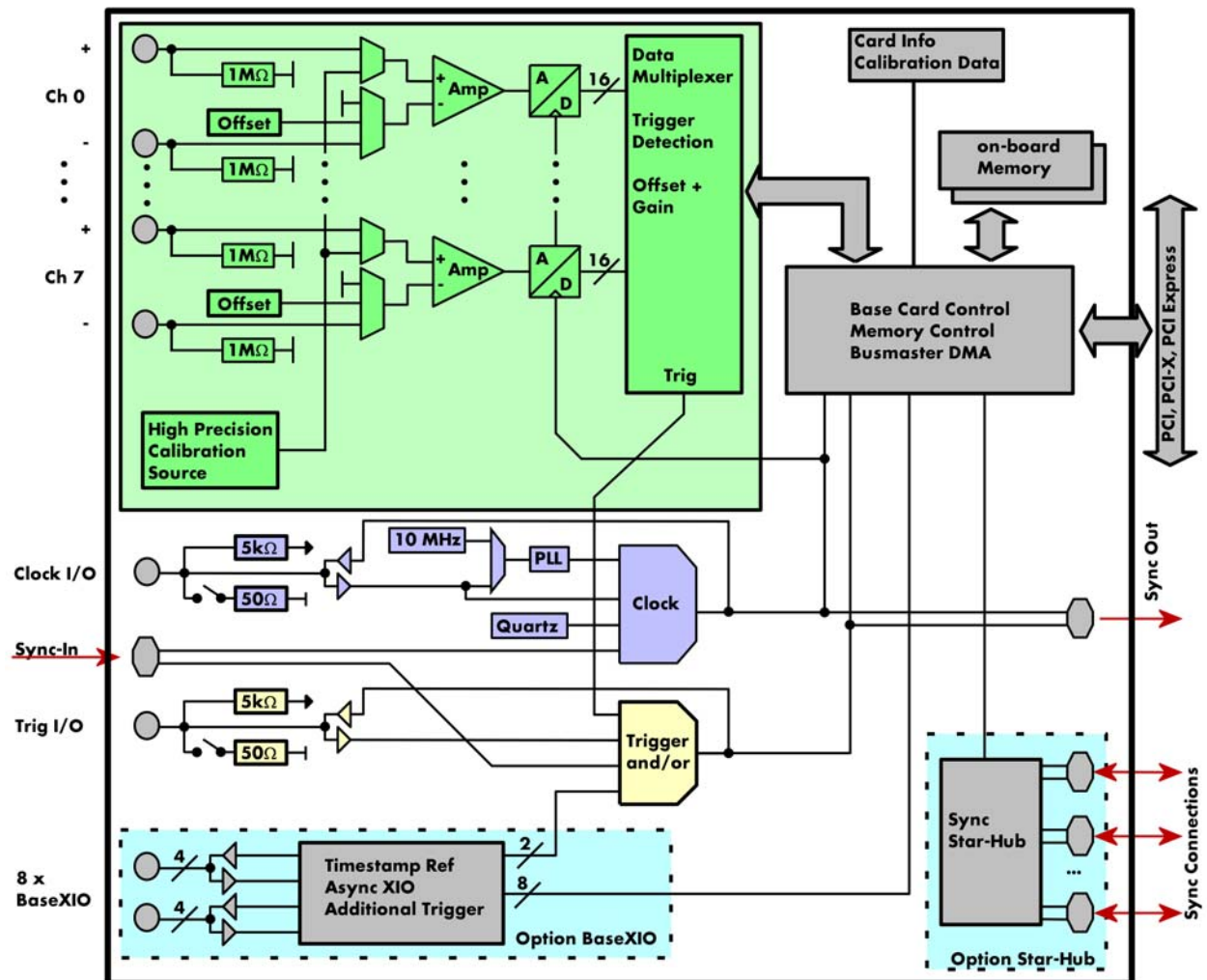
EMC Immunity	Compliant with CE Mark
EMC Emission	Compliant with CE Mark
Product warranty	2 years starting with the day of delivery
Software and firmware updates	Life-time, free of charge
MTBF	80000 hours

Dynamic Parameters

	M2i.4620	M2i.4621 M2i.4622	M2i.4630	M2i.4631 M2i.4632	M2i.4640	M2i.4641 M2i.4642	M2i.4650	M2i.4651 M2i.4652
max internal clock	200 kS/s		500 kS/s		1 MS/s		3 MS/s	
min external clock (special clock mode)	DC (DC)		DC (DC)		1 kS/s (DC)		1 kS/s (DC)	
max external clock (special clock mode)	200 kS/s (200 kS/S)		500 kS/s (500 kS/s)		1 MS/s (800 kS/s)		3 MS/s (2 MS/s)	
-3 dB bandwidth	>100 kHz		>250 kHz		>500 kHz		>1.5 MHz	
Zero noise level (Range $\geq \pm 500$ mV)	< 0.8 LSB rms		< 0.9 LSB rms		< 1.1 LSB rms		< 3.0 LSB rms	
Zero noise level (Range < ± 500 mV)	< 8 μ V rms		< 10 μ V rms		< 17 μ V rms		< 30 μ V rms	
Test - sampling rate	200 kS/s		500 kS/s		1 MS/s		3 MS/s	
Test signal frequency	10 kHz		10 kHz		10 kHz		10 kHz	
SNR (typ)	91.8 dB	91.5 dB	91.2 dB	91.0 dB	91.0 dB	90.7 dB	84.0 dB	82.5 dB
THD (typ)	-102.0 dB	-101.7 dB	-101.8 dB	-101.6 dB	-101.5 dB	-100.8 dB	-94.5 dB	-90.1 dB
SFDR (typ), excl. harm.	112.0 dB	111.5 dB	112.0 dB	111.5 dB	112.0 dB	111.2 dB	107.0 dB	105.5 dB
ENOB (based on SNR)	15.0 bit	14.9 bit	14.9 bit	14.8 bit	14.8 bit	14.7 bit	13.6 bit	13.4 bit
ENOB (based on SINAD)	14.9 bit	14.8 bit	14.8 bit	14.7 bit	14.7 bit	14.6 bit	13.5 bit	13.3 bit

Dynamic parameters are measured at ± 5 V input range (if no other range is stated) and 1 MOhm termination with the sampling rate specified in the table. Measured parameters are averaged 20 times to get typical values. Test signal is a pure sine wave of the specified frequency with > 99% amplitude. SNR and RMS noise parameters may differ depending on the quality of the used PC. SNR = Signal to Noise Ratio, THD = Total Harmonic Distortion, SFDR = Spurious Free Dynamic Range, SINAD = Signal Noise and Distortion, ENOB = Effective Number of Bits. For a detailed description please see application note 002.

Hardware block diagram



Order Information

PCI/PCI-X PCI Express

Order no. PCI/PCI-X	Order no. PCI Express	Standard mem	1 channel	2 channels	4 channels	8 channels
M2i.4620	M2i.4620-exp	128 MSample	200 kS/s	200 kS/s		
M2i.4621	M2i.4621-exp	128 MSample	200 kS/s	200 kS/s	200 kS/s	
M2i.4622	M2i.4622-exp	128 MSample	200 kS/s	200 kS/s	200 kS/s	200 kS/s
M2i.4630	M2i.4630-exp	128 MSample	500 kS/s	500 kS/s		
M2i.4631	M2i.4631-exp	128 MSample	500 kS/s	500 kS/s	500 kS/s	
M2i.4632	M2i.4632-exp	128 MSample	500 kS/s	500 kS/s	500 kS/s	500 kS/s
M2i.4640	M2i.4640-exp	128 MSample	1 MS/s	1 MS/s		
M2i.4641	M2i.4641-exp	128 MSample	1 MS/s	1 MS/s	1 MS/s	
M2i.4642	M2i.4642-exp	128 MSample	1 MS/s	1 MS/s	1 MS/s	1 MS/s
M2i.4650	M2i.4650-exp	128 MSample	3 MS/s	3 MS/s		
M2i.4651	M2i.4651-exp	128 MSample	3 MS/s	3 MS/s	3 MS/s	
M2i.4652	M2i.4652-exp	128 MSample	3 MS/s	3 MS/s	3 MS/s	3 MS/s

Memory

Order no.	Option
M2i.xxxx-256MS	Memory upgrade to 256 MSample (512 MB) total memory
M2i.xxxx-512MS	Memory upgrade to 512 MSample (1 GB) total memory
M2i.xxxx-1GS	Memory upgrade to 1 GSsample (2 GB) total memory
M2i.xxxx-2GS	Memory upgrade to 2 GSsample (4 GB) total memory

Options

Order no.	Option
M2i.xxxx-mr	Option Multiple Recording
M2i.xxxx-mgt	Option pack including Multiple Recording, Gated Sampling, Timestamp
M2i.xxxx-mgtab	Option pack including Multiple Recording, Gated Sampling, Timestamp, ABA mode
M2i.xxxx-SHS (1)	Synchronization Star-Hub for up to 5 cards, only 1 slot width
M2i.xxxx-SH16 (1)	Synchronization Star-Hub for up to 16 cards
M2i.xxxx-SSHM (1)	System-Star-Hub Master for up to 15 cards in the system and up to 17 systems, sync cables included
M2i.xxxx-SSHS5 (1)	System-Star-Hub Slave for up to 5 cards in one system, all sync cables included
M2i.xxxx-SSHS16 (1)	System-Star-Hub Slave for up to 16 cards in one system, all sync cables included
M2i.xxxx-bxio	Option BaseXIO: 8 digital I/O lines usable as asynchronous I/O, timestamp ref-clock and additional external trigger lines, additional bracket with 8 SMB connectors
M2i-upgrade	Upgrade for M2i.xxxx: later installation of option -dig or -bxio

Cables

Order no.	Option
Cab-1m-9m-80	Adapter cable MMCX male to BNC male, 80 cm (for analog inputs)
Cab-1m-9f-80	Adapter cable MMCX male to BNC female, 80 cm (for analog inputs)
Cab-1m-9m-200	Adapter cable MMCX male to BNC male, 200 cm (for analog inputs)
Cab-1m-9f-200	Adapter cable MMCX male to BNC female, 200 cm (for analog inputs)
Cab-1m-9f-5	Adapter cable MMCX male to BNC female, 5 cm (short cable especially for oscilloscope probes)
Cab-3f-9m-80	Adapter cable SMB female to BNC male, 80 cm (for clock and trigger I/O)
Cab-3f-9f-80	Adapter cable SMB female to BNC female, 80 cm (for clock and trigger I/O)
Cab-3f-3f-80	Adapter cable SMB female to SMB female, 80 cm (for clock and trigger I/O)
Cab-3f-9m-200	Adapter cable SMB female to BNC male, 200 cm (for clock and trigger I/O)
Cab-3f-9f-200	Adapter cable SMB female to BNC female, 200 cm (for clock and trigger I/O)
Cab-3f-3f-200	Adapter cable SMB female to SMB female, 200 cm (for clock and trigger I/O)

Drivers

Order no.	Option
M2i.xxxx-ml	MATLAB driver for all M2i and M2i Express cards
M2i.xxxx-lv	LabVIEW driver for all M2i and M2i Express cards
M2i.46xx-dl	DASYLab driver for all M2i.46xx cards
M2i.46xx-vee	Agilent VEE driver for all M2i.46xx cards

SBench6

Order no.	Option
SBench6	Base version which support standard mode for one card
SBench6-Pro	Professional version for one card: FIFO mode, export/import, calculation functions
SBench6-Multi	Option multiple cards: needs Professional version. Handles multiple synchronized cards in one system.
Volume Licenses	Please ask Spectrum for details.

(1) : Just one of the options can be installed on a card at a time.

(2) : Third party product with warranty differing from our export conditions. No volume rebate possible.

Technical changes and printing errors possible